REMARKS

This paper is responsive to the Final Office Action mailed on April 13, 2005. Claims 1-8, 10-18, and 20 were examined and rejected. Applicants thank the Examiner for a detailed and thoughtful examination of all the claims.

Claims 1-8, 11, and 13-18 remain in this application. Claim 1, 11, and 17 are currently amended. Claims 10, 12, and 20 are canceled without prejudice or disclaimer.

Claim Rejections – 35 U.S.C. §102(b)

Claims 1-8, 11, and 13-18 stand rejected under 35 U.S.C. §102(b) as being anticipated by Tsai (USPAP 2002/0130703).

Regarding independent claims 1, 11, and 17, Applicants have amended each of the claims to incorporate limitations that:

> *the first former-stage clock low level is shorter in time than the first clock low level and is completely covered in time within the first clock low level, and*
>
> *the second clock high level is shorter in time than the second former-stage clock high level and is completely covered in time within the second former-stage clock high level.*

Such limitations, either in part or as a whole, are not disclosed or suggested by Tsai.

As pointed out by the Examiner, Tsai discloses only **TWO** distinguishable clocks (Vphi1 and Vphi2). However, each of the independent claims 1, 11, and 17 includes at least **FOUR** distinguishable clocks, i.e., a first former-stage clock signal (PCLK1), a second former-stage clock signal (PCLK2), a first clock signal (PCLK3), and a second clock signal (PCLK4), each individually and definitely stated in the claim language as amended and even before any amendments are submitted.

The first former-stage clock (PCLK1) and the second former-stage clock (PCLK2) are non-overlapping in time with respect to each other. The first clock (PCLK3) and the second clock (PCLK4) are non-overlapping in time with respect to each other. The first former-stage clock low level of the first former-stage clock

signal (PCLK1) is shorter in time than the first clock low level of the first clock signal (PCLK3). Also, the first former-stage clock low level is completely covered in time within the first clock low level. Moreover, the second clock high level of the second clock signal (PCLK4) is shorter in time than the second former-stage clock high level of the second former-stage clock signal (PCLK2). Also, the second clock high level is completely covered in time within the second former-stage clock high level.

Neither Tsai nor the prior art made of record in the Final Office Action discloses or suggests such limitations relating to the four distinguishable clocks (PCLK1 to PCLK4) claimed by Applicants. Each of the independent claims 1, 11, and 17 is thus believed to be allowable over the art of record, and the claims dependent therefrom are likewise believed to be allowable at least for this reason.

Summary

In summary, claims 1-8, 11, and 13-18 are in the case. All of the claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Should any issues remain, Applicants respectfully requests a telephonic interview with the Examiner to discuss this response, and further in the hope that the remaining issues might be efficiently resolved.

Sincerely yours,

Winston Hsu Date: JUN 01 2005

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)